

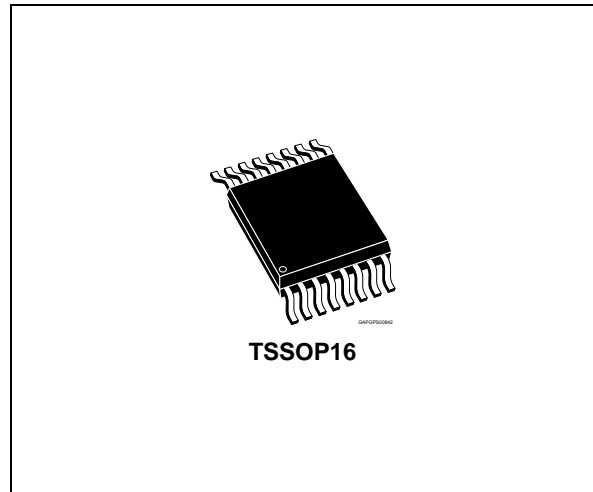
Single chip RDS demodulator

Features

- Very high RDS demodulation quality with improved digital signal processing
- High performance, 57 kHz bandpass filter (8th order)
- Filter adjustment free and without external components
- Purely digital RDS demodulation without external components
- RDS signal quality output
- 4.332 MHz crystal oscillator (8.664 MHz optional)
- Low noise cmos technology
- Low radiation

Description

The TDA7478 recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting stations and operates in accordance with the EBU (European Broadcasting Union) specifications.



The device is made up of two sections: a cascaded antialiasing + switched capacitors 8th bandpass filter for precise RDS band selection and a demodulating section that performs the extraction of RDS data stream (RDDA) and clock (RDCL), to be further processed by a suitable RDS decoder.

Output for RDS signal quality is also present.

Table 1. Device summary

| Order code | Package | Packing |
|---------------|---------|---------------|
| E-TDA7478AD | TSSOP16 | Tube |
| E-TDA7478ADTR | | Tape and reel |

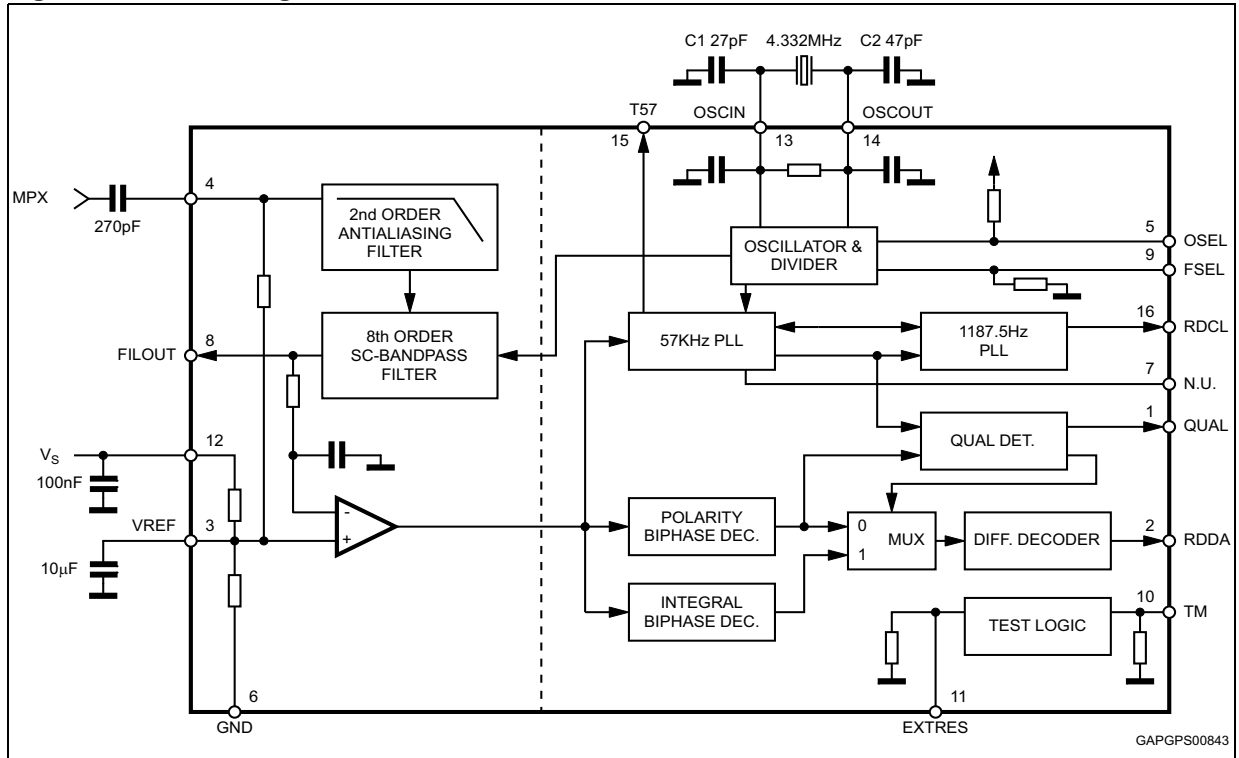
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1 Block diagram and pins description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pins description

Figure 2. Pin connection (top view)

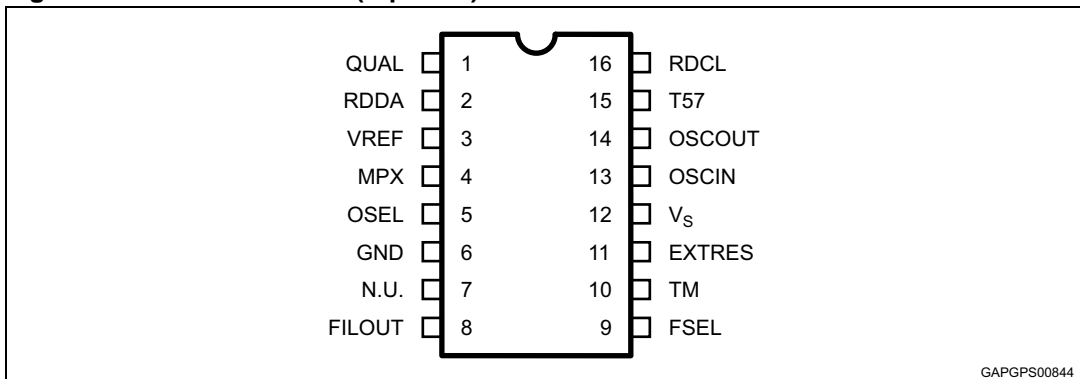


Table 2. Pins description

| Pin # | Name | Description |
|-------|--------|--------------------------------------------------------------------------------------------------------------|
| 1 | QUAL | Output for signal quality indication (High = good) |
| 2 | RDDA | RDS data output |
| 3 | VREF | Reference voltage |
| 4 | MPX | RDS input signal |
| 5 | OSEL | Oscillator selector pin: – open, closed to V_S = quartz oscillator – closed to GND = external driven |
| 6 | GND | Ground |
| 7 | N.U. | Not Used (to be left open) |
| 8 | FILOUT | Filter output |
| 9 | FSEL | Frequency selector pin: – open = 4.332 MHz – closed to V_S = 8.664 MHz |
| 10 | TM | Test mode pin: – open = normal operation – closed to V_S = testmode |
| 11 | EXTRES | Reset pin: – open = run mode – closed to V_S = reset condition |
| 12 | V_S | Supply voltage |
| 13 | OSCIN | Oscillator input |
| 14 | OSCOUT | Oscillator output |
| 15 | T57 | Testing output pin: 57 kHz clock output |
| 16 | RDCL | RDS clock output 1187.5 Hz |

2 Electrical specifications

2.1 Thermal data

Table 3. Thermal data

| Symbol | Description | Value | Unit |
|------------------|-------------------------------------|----------|---------------|
| $R_{th\ j-case}$ | Thermal resistance junction-to-case | Max. 200 | $^{\circ}C/W$ |

2.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------|-----------------------------|------------|-------------|
| V_S | Supply voltage | -0.3 to 7 | V |
| T_{op} | Operating temperature range | -40 to 85 | $^{\circ}C$ |
| T_{stg} | Storage temperature | -55 to 150 | $^{\circ}C$ |

2.3 Electrical characteristics

$T_{amb} = 25^{\circ}C$, $V_S = 5V$, unless otherwise specified.

Table 5. Electrical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------------|---------------------------|-------------------------------------------------------------------------------|------|------|------------|--------------------------|
| V_S | Supply voltage | - | 4.5 | 5 | 5.5 | V |
| I_S | Supply current | - | - | 7.5 | 12.0 | mA |
| Filter | | | | | | |
| f_C | Center frequency | - | 56.6 | 57 | 57.4 | kHz |
| BW | 3 dB bandwidth | - | 2.5 | 3 | 3.5 | kHz |
| G | Gain | $f = 57\text{ kHz}$ | 17 | 20 | 23 | dB |
| A | Attenuation | $\Delta f \pm 4\text{ kHz}$ | - | 22 | - | dB |
| | | $f = 38\text{ kHz}$ | - | 60 | - | dB |
| | | $f = 67\text{ kHz}$ | - | 45 | - | dB |
| R_I | Input impedance of MPX | - | - | 120 | - | $K\Omega$ |
| R_L | Load impedance on FILOUT | - | 1 | - | - | $M\Omega$ |
| S/N | Signal to noise ratio | $V_{IN} = 3\text{ mVRMS}$ | 30 | 40 | - | dB |
| V_{IN} | MPX input signal | $f = 19\text{ kHz}; T_3 \leq 40\text{ dB}^{(1)}$ $f = 57\text{ kHz (RDS)}$ | - | - | 1000 50 | mV_{RMS} mV_{RMS} |
| S_{RDS} | RDS detection sensitivity | - | 1 | - | - | mV_{rms} |

Table 5. Electrical characteristics (continued)

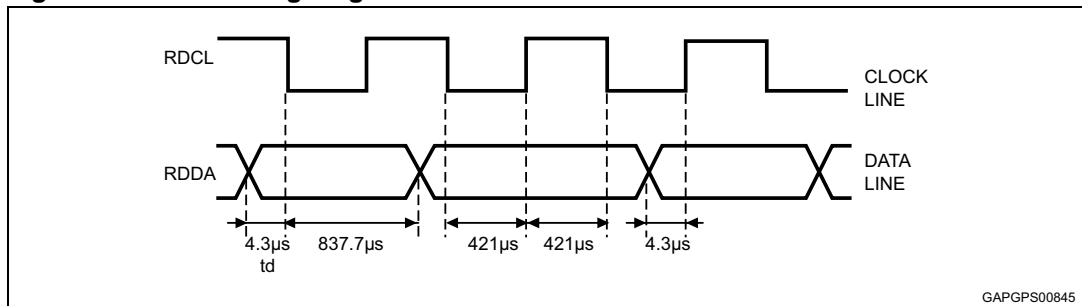
| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------------------------------------------------------------------|-----------------------------------------|-----------------------------------------|-----------------|-----------------|-----------------|---------------|
| S_{ARI} | ARI detection sensitivity | - | 3 | - | - | mVrms |
| V_{REF} | Reference | - | - | $V_S/2$ | - | V |
| Demodulator | | | | | | |
| Input pins (EXTRES, FSEL, TM) all with internal pull down resistor | | | | | | |
| Input pin (OSEL) with internal pull up resistor | | | | | | |
| I_{PD} | Input current | $V_{IN} = 5\text{ V}$ (pull-down input) | 15 | - | 30 | μA |
| I_{PU} | Input current | $V_{IN} = 0\text{ V}$ (pull-up input) | -25 | - | -10 | μA |
| V_{IH} | Input voltage high | - | $0.7 \cdot V_S$ | $0.8 \cdot V_S$ | - | V |
| V_{IL} | Input voltage low | - | - | $0.2 \cdot V_S$ | $0.3 \cdot V_S$ | V |
| Output pins (RDCL, RDDA, QUAL, T57) | | | | | | |
| V_{OH} | Output voltage high | $I_L = 0.5\text{ mA}$ | 4 | 4.6 | - | V |
| V_{OL} | Output voltage low | $I_L = 0.5\text{ mA}$ | - | 0.4 | 1 | V |
| Oscillator | | | | | | |
| V_{CLL} | Input level OSCIN pin | OSEL = open circuit | - | - | 1 | V |
| V_{CLH} | Input level OSCIN pin | OSEL = open circuit | 4 | - | - | V |
| | Amplitude OSCOUT | OSEL = open circuit | - | 4.5 | - | V |
| V_{PP} | Amplitude OSCIN (for external drive) | OSEL = GND, $f = 4.332\text{ MHz}$ | - | 100 | - | mVpp |
| | | OSEL = GND, $f = 8.664\text{ MHz}$ | - | 120 | - | mVpp |

1. The 3rd harmonic (57 kHz) must be less than -40 dB with respect to the input signal plus gain.

3 Output timing

The RDS (1187.5Hz) output clock on RDCL line is synchronized to the incoming data. According to the internal PLL lock condition data change can result on the falling or on the rising clock edge. (see [Figure 3](#)). Whichever clock edge is used by the decoder (rising or falling edge) the data will remain valid for 416.7 μ s after the clock transition.

Figure 3. RDS timing diagram



4 Oscillator controls (FSEL, OSEL)

Two different crystal frequencies can be used. The adaption of the internal clock divider to the external crystal is achieved via the input pin FSEL. See the following table for reference.

Table 6. Crystal frequencies

| Crystal | FSEL (pin configuration) |
|----------|--------------------------|
| 4.332MHz | connected to GND or open |
| 8.664MHz | connected to Vs |

A special mode is introduced to reduce EMI. With pin OSEL connected to GND the internal oscillator is switched off and an external sinusoidal frequency could be applied on OSCIN. The peak to peak voltage of this signal can be reduced down to 60 mV.

In this mode the frequency selection via FSEL is still active.

Suggested values of C1 and C2 are shown in the following table.

Table 7. C1 and C2 suggested value

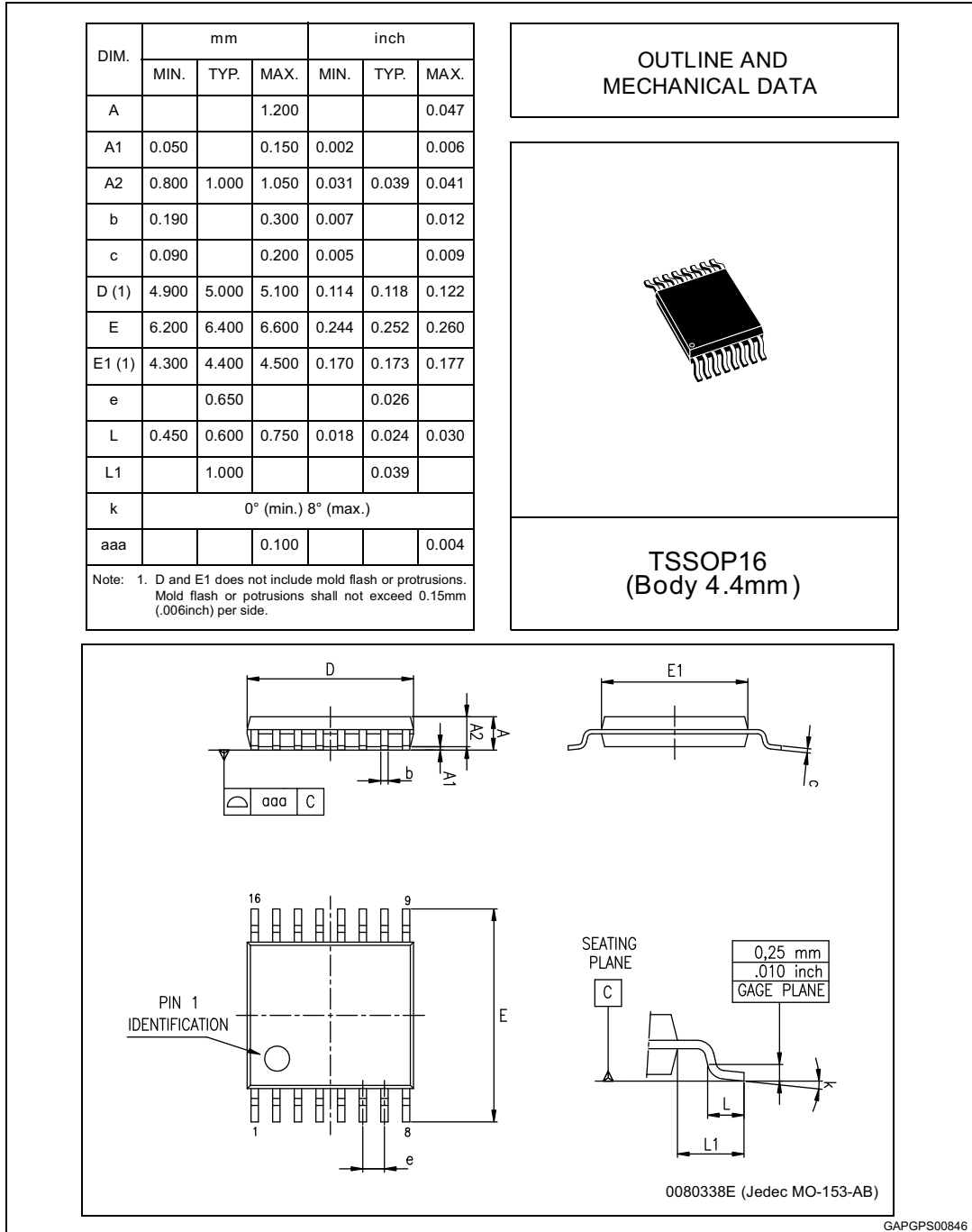
| Crystal | C1 | C2 |
|----------|------|------|
| 4.332MHz | 27pF | 47pF |
| 8.664MHz | 27pF | - |

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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Figure 4. TSSOP16 mechanical data and package dimensions



6 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|-------------|----------|----------------------------------------------------------------------------------------------------|
| 09-Jul-2004 | 1 | Initial release. |
| 14-Nov-2004 | 2 | Add in the Table 5 "RDS and ARI Detection Sensitivity" parameters. |
| 30-Jun-2011 | 3 | Document reformatted. Updated order code in Table 1: Device summary on page 1 . |
| 23-Sep-2013 | 4 | Updated Disclaimer. |

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