dsPIC33FJ12MC201/202 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ12MC201/202 family devices that you have received conform functionally to the current Device Data Sheet (DS70265**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ12MC201/202 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 11, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ12MC201/202 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A2	A3	A4	A5
dsPIC33FJ12MC201	0x0800	0x3001	0x3002	0x3003	0x3005
dsPIC33FJ12MC202	0x0801				

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A2	A3	A4	A5
JTAG	Flash Programming	1.	JTAG programming does not work.	X	X	X	X
UART	High-Speed Mode	2.	UART receptions may be corrupted if the Baud Rate Generator (BRG) is set up for 4x mode.	X	X	X	X
UART	High-Speed Mode	3.	The auto-baud feature may not calculate the correct baud rate when the BRG is set up for 4x mode.	X	X	X	X
UART	Auto-Baud	4.	With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.	X	X	X	X
UART	Auto-Baud	5.	The auto-baud feature measures baud rate inaccurately for certain baud rate and clock speed combinations.	X	X	X	X
UART	Auto-Baud	6.	When an auto-baud is detected, the receive interrupt may occur twice.	X	X	X	X
UART	High-Speed Mode	7.	When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.	X	X	X	X
UART	IR Mode	8.	The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.	X	X	X	X
Interrupt Controller	Idle Mode	9.	If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine (TSR).	X	X	X	X
SPI	SCKx Pins	10.	The SPIxCON1 DISSCK bit does not influence port functionality.	X	X	X	X
I^2C™™	SFR Writes	11.	The BCL bit in I2CSTAT can only be cleared with a 16-bit operation, and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.	X	X	X	X
I^2C	10-bit Addressing	12.	When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.	X	X	X	X
Product Identification	Extended Temperature	13.	Revision A2 devices marked as extended temperature range (E) devices only support industrial temperature range (I).	X			
UART	Interrupts	14.	The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.	X	X	X	X
UART	IR Mode	15.	When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA® encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.	X	X	X	X
Internal Voltage Regulator	Sleep Mode	16.	When the VREGS bit (RCON<8>) is set to a logic '0', device may Reset and higher sleep current may be observed.	X	X	X	X
PSV Operations	—	17.	An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.	X	X	X	X
I^2C	10-bit Addressing	18.	When the I^2C module is configured as a 10-bit slave with an address of 0x02, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A2	A3	A4	A5
I^2C	—	19.	With the I^2C module enabled, the port bits and external interrupt input functions (if any) associated with SCL and SDA pins do not reflect the actual digital logic levels on the pins.	X	X	X	X
I^2C	10-bit Addressing	20.	The 10-bit slave does not set the RBF flag or load the I2CxRCV register on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.	X	X	X	X
I^2C	—	21.	After the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.	X	X	X	X
CPU	EXCH Instruction	22.	The EXCH instruction does not execute correctly.	X	X	X	X
PWM	Debug Mode	23.	PTMR does not keep counting down after halting code execution in Debug mode.	X	X	X	X
PWM	DOZE Mode	24.	The Motor Control PWM module generates more interrupts than expected when DOZE mode is used and the output postscaler value is different than 1:1.	X	X	X	X
QEI	Interrupts	25.	The QEI module does not generate an interrupt in a particular overflow condition.	X	X	X	X
UART	Break Character Generation	26.	The UART module will not generate back-to-back Break characters.	X	X	X	X
QEI	Timer Gated Accumulation Mode	27.	When Timer Gated Accumulation is enabled, the QEI does not generate an interrupt on every falling edge.	X	X	X	X
QEI	Timer Gated Accumulation Mode	28.	When Timer Gated Accumulation is enabled, and an external signal is applied, the POSCNT increments and generates an interrupt after a match with MAXCNT.	X	X	X	X
SPI	Slave FRMDLY	29.	The SPI communication in Framed mode does not function correctly if the Slave SPI frame delay bit (FRMDLY) is set to ‘1’.	X	X	X	X
ADC	Current Consumption in Sleep Mode	30.	If the ADC module is in an enabled state when the device enters Sleep mode, the power-down current (I_{PD}) of the device may exceed the device data sheet specifications.	X	X	X	X
CPU	`div.sd`	31.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X	X	X	X
UART	TX Interrupt	32.	A transmit (TX) Interrupt may occur before the data transmission is complete.	X	X	X	X
JTAG	Flash Programming	33.	JTAG Flash programming is not supported.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: JTAG

JTAG programming does not work.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

2. Module: UART

UART receptions may be corrupted if the Baud Rate Generator is set up for 4x mode (BRGH = 1).

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

3. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRGH, is set. With the BRGH bit set, the baud rate calculation used is the same as BRG = 0.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRGH bit.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

4. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

5. Module: UART

The auto-baud feature may miscalculate certain baud rate and clock speed combinations, resulting in a BRG value that is greater than or less than the expected value by 1. This may result in reception or transmission failures.

Work around

Test the auto-baud rate at various clock speed and baud rate combinations that would be used in an application. If an inaccurate BRG value is generated, manually correct the baud rate in user software.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

6. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If an extra interrupt is detected, ignore the additional interrupt.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

7. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

8. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

9. Module: Interrupt Controller

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled) the user software should check the state of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred, and then perform the appropriate clock switch operation. Regardless, the Trap Service Routine must be included in the user application.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

10. Module: SPI

Setting the DISSCK bit in the SPIxCON1 register does not allow the user application to use the SCK pin as a General Purpose I/O pin.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

11. Module: I²C™

The BCL bit in I2CSTAT can be cleared only with a 16-bit operation, and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

Work around

Use 16-bit operations to clear BCL.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

12. Module: I²C

If there are two I²C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I²C devices, the addresses as well as bits A10 and A9 should be different.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

13. Module: Product Identification

Revision A2 devices marked as extended temperature range (E) devices only support industrial temperature range (I).

Work around

Use Revision A3 or newer devices marked as extended temperature range (E) devices.

Affected Silicon Revisions

A2	A3	A4	A5				
X							

14. Module: UART

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

15. Module: UART

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

16. Module: Internal Voltage Regulator

When the VREGS bit (RCON<8>) is set to a logic '0', the device may Reset and a higher sleep current may be observed.

Work around

Ensure VREGS bit (RCON<8>) is set to a logic '1' for device Sleep mode operation.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

17. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This occurs only when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

18. Module: I^2C

When the I^2C module is configured as a 10-bit slave with an address of 0x02, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

19. Module: I^2C

With the I^2C module enabled, the port bits and external interrupt input functions (if any) associated with the SCL and SDA pins do not reflect the actual digital logic levels on the pins.

Work around

If the SDA and/or SCL pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I^2C module.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

20. Module: I²C

In 10-bit Addressing mode, some address matches do not set the RBF flag or load the receive register, I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

21. Module: I²C

When the I²C module is operating in either Master or Slave mode, after the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

22. Module: CPU

The EXCH instruction does not execute correctly.

Work around

If writing source code in assembly, the recommended work around is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
MOV Wsource, Wdestination
POP Wsource
```

If using the MPLAB C30 C compiler, specify the compiler option: `-merrata=exch` (*Project > Build Options > Projects > MPLAB C30 > Use Alternate Settings*).

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

23. Module: PWM

If the PTDIR bit is set (when PTMR is counting down), and the CPU execution is halted (after a breakpoint is reached), PTMR will start counting up as if PTDIR was zero.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

24. Module: PWM

When the device is operated in DOZE mode and the Motor Control PWM module has a postscaler set to any value different than 1:1 (PTOPS > 0 in PxTCON register), the Motor Control PWM module generates more interrupts than expected.

Work around

Do not use DOZE mode with the Motor Control PWM if the time base output postscaler is different than 1:1 (PTOPS > 0 in PxTCON register).

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

25. Module: QEI

The Quadrature Encoder Interface (QEI) module does not generate an interrupt when MAXCNT is set to 0xFFFF and the following events occur:

1. POSCNT underflows from 0x0000 to 0xFFFF.
2. POSCNT stops.
3. POSCNT overflows from 0xFFFF to 0x0000.

This sequence of events occurs when the motor is running in one direction, which causes POSCNT to underflow to 0xFFFF. Then, if the motor stops and starts running in the opposite direction an overflow from 0xFFFF to 0x0000 will be generated. The QEI module does not generate an interrupt when this condition occurs.

Work around

To prevent this condition from occurring, set MAXCNT to 0x7FFF, which will cause an interrupt to be generated by the QEI module.

In addition, a global variable could be used to monitor bit 15, so that when an overflow or underflow condition is present on POSCNT, the variable will toggle bit 15. Example 1 shows the code required for this global variable.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

26. Module: UART

The UART module will not generate consecutive break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

EXAMPLE 1:

```
unsigned int POSCNT_b15 = 0;
unsigned int Motor_Position = 0;

int main(void)
{
            // ... User's code

            MAXCNT = 0x7FFF;       // Instead of 0xFFFF

            Motor_Position = POSCNT_b15 + POSCNT;

            // ... User's code
}
void __attribute__((__interrupt__)) _QEIInterrupt(void)
{
            IFSxbits.QEIIF = 0;    // Clear QEI interrupt flag
                                   // x=2 for dsPIC30F
                                   // x=3 for dsPIC33F
            POSCNT_b15 ^= 0x8000;  // Overflow or Underflow
}
```

27. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, a QEI interrupt should be generated after an input pulse on the QEA input. This interrupt is not generated in the affected silicon.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

28. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, the POSCNT counter should not increment but erroneously does, and if allowed to increment to match MAXCNT, a QEI interrupt will be generated.

Work around

To prevent the erroneous increment of POSCNT while running the QEI in Timer Gated Accumulation mode, initialize MAXCNT = 0.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

29. Module: SPI

Regardless of the Slave setting for the Frame delay bit (FRMDLY = 0 or FRMDLY = 1), the Slave always acts as if the sync pulse precedes the first SPI data bit (FRMDLY = 0). The SPI will not function as described if Slave FRMDLY = 1.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

30. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a PWRSAV #0 instruction, the device power-down current (IPD) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work around 1:

In order to remain within the IPD specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a PWRSAV #0 instruction.

Note: The ADC module must be reinitialized by the user application before resuming ADC operation.

Work around 2:

If the ADC module was previously initialized and enabled, before entering Sleep, execute the lines of code provided in Example 2.

Note: Unlike **Work around 1**, the user application does not need to reinitialize the ADC module; however, it is necessary to re-enable the ADC module by setting the ADON bit after waking from Sleep.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

EXAMPLE 2:

```
AD1CON1bits.ADON = 0;              //Disable the ADC module
__asm__ volatile ("REPEAT #50");  //Wait 50 Tcy
__asm__ volatile ("NOP");          //Repeat NOP 51 times
Sleep();                           // Execute PWRSAV #0 and go to Sleep
```

31. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

32. Module: UART

When using UTXISEL = `01` (Interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) Interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete. Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

33. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70265**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

The maximum value for parameter DI19 (V_{IL} specifications for SDAx and SCLx pins) was stated incorrectly in Table 24-9 of the current device data sheet. Also, parameters DI28 and DI29 (V_{IH} specifications for SDAx and SCLx pins) were not stated. The correct values are shown in bold type in Table 24-9.

TABLE 24-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
	V_{IL}	Input Low Voltage					
DI18		**SDAx, SCLx**	V_{SS}	—	0.3 V_{DD}	V	SMBus disabled
DI19		**SDAx, SCLx**	V_{SS}	—	**0.8**	V	SMBus enabled
	V_{IH}	Input High Voltage					
DI28		**SDAx, SCLx**	**0.7 V_{DD}**	**—**	**5.5**	**V**	**SMBus disabled**
DI29		**SDAx, SCLx**	**2.1**	**—**	**5.5**	**V**	**SMBus enabled**

2. Module: Electrical Characteristics

The temperature range for parameter F20a (Internal FRC accuracy) was stated incorrectly in Table 24-18 of the current device data sheet. The correct values are shown in bold type in Table 24-18.

TABLE 24-18: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	Internal FRC Accuracy @ 7.3728 MHz(1)						
F20a	FRC	-2	—	+2	%	**0°C ≤ TA ≤ +85°C**	V_{DD} = 3.0-3.6V
F20b	FRC	-5	—	+5	%	-40°C ≤ TA ≤ +125°C	V_{DD} = 3.0-3.6V

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits may be used to compensate for temperature drift.

APPENDIX A: REVISION HISTORY

Rev A Document (4/2009)

Initial release of this document; issued for revision A2, A3 and A4 silicon.

Includes silicon issues 1 (JTAG), 2-8 (UART), 9 (Interrupt Controller), 10 (SPI), 11-12 (I^2C™), 13 (Product Identification), 14-15 (UART), 16 (Internal Voltage Regulator), 17 (PSV Operations), 18-21 (I^2C), 22 (CPU), 23-24 (PWM) and 25 (QEI).

This document replaces the following errata document:

DS80328, *"dsPIC33FJ12MC201/202 Rev. A2/A3/A4 Silicon Errata"*

Rev B Document (8/2009)

Added silicon issues 26 (UART) and 27-28 (QEI).

Rev C Document (1/2010)

Added silicon issue 29 (SPI).

Rev D Document (6/2010)

Updated silicon issue 22 (CPU).

Added references to revision A5 silicon throughout the document.

Added silicon issue 30 (ADC) and data sheet clarification 1 (Electrical Characteristics).

Rev E Document (10/2010)

Updated the work around in silicon issue 30 (ADC).

Rev F Document (11/2011)

Added silicon issues 31 (CPU), 32 (UART), and 33 (JTAG).

Rev G Document 5/2012

Added data sheet clarification 2 (Electrical Characteristics) and updated typographic formatting in data sheet clarification 1 (Electrical Characteristics).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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